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EXAMINER	
STEVENS, THOMAS H	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 03/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/754,406	XU, SONGJIE	
	Examiner	Art Unit	
	Mary C Hogan	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11/29/04*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11,13-29 and 31-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11, 13-29, 31-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 November 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/29/04*.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This application has been examined.

2. Claims 1-31 have been examined and rejected.

Response to Amendment and 35 USC § 112 Rejection

3. Upon reexamination of the substitute specification filed June 21, 2002 and in light of Applicant's amendment to the substitute specification filed November 29, 2004, the claim rejections under 35 USC § 112, first paragraph have been removed. It was determined that the portions added to the specification were not the basis for any claim limitations.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. **Claims 1-10, 25-28, 32-34** are rejected under 35 U.S.C. 102(b) as being anticipated by Singh (Singh, K.J., "Performance Optimization of Digital Circuits, Ph.D. Dissertation, University of California Berkley, 1992), herein referred to as **Singh '92**.

6. As to **Claim 1**, **Singh '92** teaches a method of reducing circuit timing delays comprising

selecting a first node **(section 3.2.1, first paragraph, O1 as "most critical output"; page 57, first paragraph, "x")**

sorting fanins of the first node according to slack values associated with the corresponding fanins, wherein at least a portion of the slack values differ in value **(section 3.2.1, second sentence; page 57, "...in a tree, the slack is non-decreasing along any path from input to output. This implies that for a node y that is a fanin of node x, $s(x) \leq s(y)$")**

reducing delays associated with fanins having relatively larger negative slack values before reducing delays associated with fanins having relatively smaller negative slack values **(page 60, HEURISTIC-2, sentences 1-6; page 60-61, HEURISTIC-3, sentences 1-2).**

7. As to **Claims 2 and 3, Singh '92** teaches reducing delays performed recursively wherein recursively reducing delays is performed until delays cannot be further reduced or timing constraints are violated **(Figure 3.5; page 60, HEURISTIC-1, "...several iterations may be required to meet the achievable target s*).**

8. **As to Claim 4, Singh '92** teaches selecting the first node comprising
performing a timing analysis on a circuit **(equation 3.1)**
determining a delay target based at least in part on the timing analysis **(equation 3.2, s*)**
determining a slack value for each critical node of the circuit based on the delay target **(Figure 3.6 and description)**
sorting the critical nodes based on the corresponding slack values **(Figure 3.7 and pages 48-49, description of ε-critical network,** wherein the slack values of the nodes determine whether or not they are in the ε-critical network)

9. As to **Claim 5, Singh '92** teaches selecting the first node further comprising selecting a critical node having the largest negative slack **(page 49, "most critical output, O_1").**

10. As to **Claim 6, Singh '92** teaches a method of reducing circuit timing delays comprising
selecting a first node **(section 3.2.1, first paragraph, O1 as "most critical output"; page 57, first paragraph, "x")**
identifying critical fanins of the first node **(page 49, description of ε-critical network; page 57, relevant path and node y)**
recursively reducing delays associated with at least a portion of the critical fanins of the first node **(page 60, HEURISTIC-2,** improving the most critical path of the circuit; page 59-61, HEURISTIC-3 wherein the transitive fanin for each output is considered as the relevant network and each critical output is targeted for delay improvement**).**

11. As to **Claim 7, Singh '92** teaches recursively reducing delays is performed on critical fanins having relatively larger negative slack values before reducing delays associated with fanins having relatively smaller negative slack values **(page 60, HEURISTIC-2, sentences 1-6; page 60-61, HEURISTIC-3, sentences 1-2).**

12. As to **Claim 8, Singh '92** teaches performing a local transformation on the first node if the reducing delays for at least one of the critical fanins is not successful **(section 3.2.1, paragraphs 1 and 2).**

13. As to **Claim 9, Singh '92** teaches a method of performing circuit delay reduction comprising
performing a timing analysis on a circuit **(equation 3.1)**

determining a delay target based at least in part on the timing analysis **(equation 3.2, s*)**

selecting a first output having a negative slack based at least in part on the delay target and the amount of first output negative slack relative to the slack of other outputs **(page 45 and page 49, "most critical output, O_1")**

performing local transformations on transitive fanins of the first output to improve the negative slack **(section 3.2.1, paragraphs 1 and 2).**

14. As to **Claim 10, Singh '92** teaches the first output is a critical output **(page 45 and page 49, "most critical output, O_1")**.

15. As to **Claim 25, Singh '92** teaches: a layout-driven logic synthesis design flow, comprising:

selecting a desired circuit delay associated with a first output of a circuit path **(page 59, description of Δ)**;

calculating an initial circuit delay associated with the first output **(Figure 3.8, computation of δ and equation 3.1; page 60, HEURISTIC-2, δ in equation forΔ)**; and

iteratively reducing the initial circuit delay to achieve the desired circuit delay using a timing optimization process, wherein in an iteration, mapping and clustering are used to measure the outcome of the timing optimization procedure, and wherein the timing optimization process uses such measurements to achieve the desired delay, and wherein the result of an iteration of delay reduction is used by a next iteration of delay reduction to determine an amount of delay to reduce **(Figure 3.11; page 60, description of HEURISTIC-2)**.

16. As to **Claims 25-28, Singh '92** teaches a method of reducing timing delays on a critical path of a circuit topology during an early stage of the design process during the optimization phase of an integrated circuit in which the design is placed and optimized for timing **(page 33, paragraph 1)**. The design of combinational logic and the following placement of this design encompass topology associated with standard cell design, gate array design and programmable logic design since these are all designs that are placed and further optimized for performance and layout area purposes.

17. As to **Claim 32, Singh '92** teaches: additionally comprising performing a local transformation on the first node if the reducing delays for at least one of a set of fanins of the first node is not successful **(section 3.2.1, paragraphs 1and 2)**.

18. As to **Claim 33, Singh '92** teaches: wherein reducing delays associated with the fanins of the first node is performed before any local transformation of the first **node (section 3.2.1, first paragraph,** specifically the last two lines, wherein a local transformation is needed since the circuit performance was virtually unchanged).

19. As to **Claim 34, Singh '92** teaches: wherein sorting fanins of the first node includes sorting fanins of the first node in order according to slack values associated with the corresponding fanins **(section 3.2.1, second sentence; page 57, "...in a tree, the slack is non-decreasing along any path from input to output. This implies that for a node y that is a fanin of node x, $s(x) \leq s(y)$")**.

20. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

21. **Claim 21-24** are rejected under 35 U.S.C. 102(b) as being anticipated by Singh et al ("Timing Optimization of Combinational Logic", ICCAD-88. Digest of Technical Papers., IEEE International Conference 7-10 Nov. 1988, Pages 282-285), herein referred to as **Singh '88**.

22. As to **Claim 21, Singh '88** teaches a method of dynamically reducing delays on a critical path of a circuit topology, the method comprising:

> identifying a critical path of the circuit topology **(Abstract, sentence 2; section 2.1, paragraph 2)**
>
> selecting a delay target for a primary output associated with the critical path **(Figure 2,** "timing constraint"**; section 2, paragraph 1)**
>
> reducing a first critical path delay beginning at a first node in closer proximity to a primary input associated with the critical path than to the primary output **(section 2.5, last paragraph)**
>
> storing the reduced delay **(section 2.5, second paragraph** last 2 sentences wherein it is described that at the arrival times at a node are updated, therefore, the decomposition of the node is adjusted dynamically to the updated delay, therefore, the updated or reduced delay must be stored for the decomposition to be adjusted**)**
>
> reducing a second critical path delay beginning at a second node located between the first node and the primary output based at least in part on the stored delay **(Figure 2,** where speedup_node is performed for each node**)**

23. As to **Claims 22-24, Singh '88** is directed to speeding up combinational logic **(Abstract, sentence 1)** wherein changes are made to the topology and layout, or placement **(Introduction, paragraph 1)** of a circuit design that uses gates **(section 2, paragraph 1)**. The design of combinational

logic and the following placement of this design **(Introduction, paragraph 1)** encompasses topology associated with standard cell design, gate array design and programmable logic design since these are all designs that are placed and further optimized for performance and layout area purposes.

24. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

25. **Claims 29 and 31** are rejected under 35 U.S.C. 102(b) as being anticipated by Huang et al, ("An Iterative Area/Performance Trade-Off Algorithm for LUT-Based FPGA Technology Mapping", Computer-Aided Design, 1996. ICCAD-96. Digest of Technical Papers., 1996 IEEE/ACM International Conference on , 10-14 Nov. 1996 Pages:13 – 17), herein referred to as **Huang**.

26. As to **Claim 29**, **Huang** teaches a method of performing a local transformation on a node in a circuit topology having at least one fanin cone and a critical fanin cone, the method comprising:

identifying a delay target for the node **(Figure 1, "Target_Level")**

collapsing the critical fanin cone for the node based on a predetermined collapse depth **(section 3, last paragraph,** in particular, sentence 3)

determining if the delay target for the node is met **(Figure 1, "if (l(Net) == Target_Level");** and

collapsing a fanin cone for the node based on the predetermined collapse depth if the delay target for the node is not met **(section 4, second paragraph, first sentence);**

setting the collapse depth to an initial value **(section 4, paragraph 3, first sentence)**; and

automaticallv changing the collapse depth to a new value if the delay target is not met **(section 4, second paragraph, first sentence)**.

27. As to **Claim 31**, **Huang** teaches performing timing-driven decomposition on the node prior to determining if the delay target is met **(Figure 1, section L2 and description)**.

Claim Rejections - 35 USC § 103

28. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

29. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

30. **Claims 35-37** are rejected under 35 U.S.C. 103(a) as being unpatentable over Singh '92 as applied to claim 1 above, and further in view of Singh et al ("A Heuristic Algorithm for the Fanout Problem", 27th ACM/IEEE Design Automation Conference, 1990), herein referred to as Singh '90.

31. As to **Claim 35, Singh '92** teaches: computing a delay target for each of the fanins **(equation 3.2, s*, Figure 3.6 and description)** and performing a delay reduction on the fanin recursively **(HEURISTIC 1-3 and descriptions)**. **Singh '92** also discloses the use of arrival and required times at nodes **(page 57)** that are used in finding a selection set that achieves a predicted delay improvement through a transformation **(page 56, 2nd to last paragraph)**.

32. **Singh '92** does not expressly teach b) determining if an arrival time for a one of the fanins is greater than the delay target for the one fanin; and c) performing a delay reduction on the one fanin reclusively if the arrival time for the one fanin is greater than the delay target for the one fanin; and repeating b) and c) for a next fanin of the first node.

33. **Singh '90** teaches an algorithm, buffer_network, wherein a) a target value is determined **(Figures 1 and 2, TR)**, b) & c) determining if an arrival time for a one of the fanins is greater than the delay target for the one fanin and performing a delay reduction on the one fanin reclusively if the arrival time for the one fanin is greater than the delay target for the one fanin **(section 2.2, first paragraph)**; and repeating b) and c) for a next fanin of the first node **(Figure 1**, "for each n" statement and "while" statement). **Singh '90** teaches this algorithm is used as part of a delay improving transformation **(Introduction, last**

paragraph, section 2.2, first sentence). Further, it is noted that **Singh'90** and **Singh '92** share the same author and further, both papers are directed to methods to reduce the delay in a circuit.

34. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the delay improvement transformations as taught in **Singh '92** to include a delay improvement transformation using a recursive algorithm such as buffer_network as taught in **Singh '90** since both **Singh '90** and **Singh '92** are directed to reducing delays of a circuit through local transformations.

35. As to **Claim 36**, **Singh '92 and Singh '90** teach: wherein reducing delays associated with the fanins of the first node further comprises stopping after c) if the delay reduction of one of the fanins is not successful **(Singh '90: section 2.2, 3rd paragraph, last 2 sentences)**.

36. As to **Claim 37**, **Singh '92 and Singh '90** teach: wherein the delay target for a particular fanin is based on a delay target of the first node, a pin-to-pin delay of the particular fanin, and an interconnect delay from the particular fanin **(Section 2.1, description of parameterized linear delay model; Figure 2)**.

37. **Claims 11-20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ju et al ("Incremental Techniques for the Identification of Statistically Sensitizable Critical Paths", 28th ACM/IEEE Design Automation Conference, Paper 32.2, pages 541-546, 1991), herein referred to as **Ju,** and further in view of **Singh '92**.

38. As to **Claim 11**, **Ju** teaches an incremental timing verification and delay reduction algorithm that selects a first critical path based on ordering the PO nodes by slack values **(section 3.1)**, incrementally identifies the next critical paths in the network **(section 3.2, paragraph 1)** and stores the delay of the next critical path **(section 3.2, paragraph 2)**. The iteration of this algorithm for successive critical paths is shown **(page 544, Algorithm: Path Enumeration)**. This algorithm is used to incrementally reduce the delay of the circuit **(Experimental Results, paragraph 1)**.

39. Although **Ju** teaches delay reduction **(Experimental Results, paragraph 1)**, he does not expressly teach determining if a delay reduction meets a predetermined criteria.

40. **Singh '92** teaches various algorithms for reducing the delay of a circuit in which algorithms are re-iterated until a timing constraint (predetermined criteria) are met (see descriptions for HEURISTICs 1-3, pages 59-62). The methods in **Singh '92** are used to reduce delay in combinational logic circuits that are described using, critical paths, critical nodes and slack values as disclosed in **Ju**.

41. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the delay reduction as taught in **Ju** to use a delay reduction algorithm as taught in Singh '92

since both **Ju** and **Singh '92** are directed to reducing the delay in combinational logic circuits taking into account critical paths, critical nodes and slack values.

42. As to **Claim 13, Singh '92** teaches the critical path is reduced in delay so as to meet a target timing constraint **(page 60, line 8 and Figure 3.5)**.

43. As to **Claim 14, Singh '92** teaches establishing the criteria **(page 60, line 8 and Figure 3.5,** wherein the timing constraint must be set in the algorithm by a user**)**.

44. As to **Claims 15-17, Singh '92** teaches a method of reducing timing delays on a critical path of a circuit topology during an early stage of the design process during the optimization phase of an integrated circuit in which the design is placed and optimized for timing **(page 33, paragraph 1)**. Since combinational logic is first designed, laid-out on the chip and subsequently mapped, it is concluded that the timing optimization process can be performed at all these phases of the design process.

45. As to **Claim 18, Singh '92** teaches the first PI node and the second PI node are the same **(page 61, Figure 3.12b paths {T,U,W,Y} and {T,Z,V,X})**.

46. As to **Claim 19, Singh '92** teaches the first PO node and the second PO node are the same **(page 61, Figure 3.12c paths {U,X} and {V,X})**.

47. As to **Claim 20, Singh '92** teaches a portion of the first critical path overlays a portion of the second critical path **(page 67, Figure 3.15, paths {S,U,V,X,Y} and {T,U,V,X,Y})**.

Response to Arguments

48. Applicant's arguments, see pages 21-25, filed 1/2/01, with respect to the rejection(s)of claim(s) 1-31 under 35 U.S.C 102(b) and 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of different interpretation of previously applied references and of new found art.

Conclusion

49. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mary C Hogan whose telephone number is 571-272-3712. The examiner can normally be reached on 7:30AM-5PM Monday-Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on 571-272-3716. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained

from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mary C. Hogan
Assistant Patent Examiner
Art Unit 2123

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